

Pattern Generator & Checker

E5020 Operation Manual

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1. General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate With Covers. Do not operate this product with covers.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Wear Eye Protection. Wear eye protection if exposure to high-intensity rays or Laser radiation exists.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Be careful in the electrostatic discharge.

2. Introduction of E5020

2.1 Primary function of E5020

E5020 can be used for the high frequency, both broad band and base band signal transmission performance test; also for pattern generation and generate multi-standard test patterns on different rate; at the same time, with different test boards, it can test BER and eye pattern characters of different Optical Modules such as SFP, GBIC, SFF, 1x9, and different Optical Components such as PIN-TIA, APD-TIA (Eye Pattern Analyzer or High Performance Oscilloscope is needed in eye pattern test). The detailed measure of test can find in Application Notes accordingly.

The multi-rate of optical module and component on the test cover the following ones: 125Mbps、155Mbps、200Mbps、622Mbps、1.0625Gbps、1.25Gbps、1.448Gbps、2.125Gbps、2.5Gbps、2.666Gbps、3.125Gbps、4.25Gbps (Option). In addition, INSTELENT can customize the test board about other rate depending on the customer's need.

E5020 can generate many kinds of pattern as follows: four PRBS are PRBS 2^7-1 , PRBS $2^{15}-1$, PRBS $2^{23}-1$ and PRBS $2^{31}-1$; K28.5 is used for mixed frequency test pattern of testing deterministic jitter; CRPAT is the compliant random pattern; CJTPAT is the compliant jitter tolerance pattern; and other high frequency, low frequency test patterns.

For test convenience, E5020 can automatically store the current state while being shut down. Further more, E5020 can store up to five state of parameter setting, which are frequently used.

2.2 Composing of E5020

The view of E5020 is shown in Figure1.



Figure 1: External view of E5020

2.3 Front panel of E5020

It is composed of screen, keyboard, channel1, and SFP interface. See the Figure2.



Figure 2: The front panel of E5020

The LCD whose type is 4x20 characters with 8x6 lattices, and LCD has backlight on/off function by choosing the menu's relative option. LCD is used for displaying the menu, the operation mode and the results of test.

There are 6 indicator lights on the front panel. Three of them are used for showing the on/off status of the CH1, CH2, SFP. Two of them are used for showing TX_FAULT and RX_LOS status of SFP. The rest one is used for denoting the normal running.

E5020 can monitor the performance of the SFP module through the TX_FAULT and RX_LOS. When SFP's transmitter has fault, the TX_FAULT signal is lightened. When SFP's receiver has fault, the RX_LOS signal is lightened.

CH1 is the current interface of test, composing with 6 SMA knots, DOUT is differential data signal out, DIN is differential data signal in, CLK is differential clock signal out.

SFP interface is compliant with the MSA. The standard can find in the following website.

<http://www.schelto.com/SFP/SFP%20MSA.pdf>

2.4 Rear panel of E5020

See the Figure3.



Figure 3: The rear panel of E5020

It is composed of the power interface, power switch, CH2 (Extended purpose), SFP clock out, USB interface (Extended purpose) and the fan.

The USB interface can connect to the computer, and then E5020 can be controlled through the computer. So you can build the automatic testing system conveniently, the diver program of serial interface will be provided by INSTELMENT, this function is an extended one.

3. Configuration of E5020

3.1 Standard configuration

There are composed of an E5020, a power cable of 220V, two RF cables with 0.8 meter length, two 50 ohm payload which are compliant with SMA standard, a CD embodied the operation manual and the application notes.

3.2 Optional configuration

The INSTELENT T5001 test board, it can be used for testing the SFP/GBIC optical module.

The INSTELENT T5002 test board, it can be used for testing the SFF2x5/ SFF2x6/ SFF2x10/ 1x9 optical module.

The INSTELENT T5003 test board, it can be used for testing the PIN-TIA/APD-TIA optical component.

The INSTELENT E5020 serial interface's driver program, it can be used for building automatic testing system.

3.3 Other clarification

The standard configuration is supplied with E5020.

If you need the item of the optional configuration, please contact INSTELENT.

4. E5020's performance

4.1 General performance

E5020 integrates the function of pattern generating and checking, it has low jitter output and can be used to demarcate the performance of optical modules and components. E5020 supports the choosing of rate from 155Mbps to 3.125Gbps (Moreover, customer can tailor the required rate.), and supports the choosing of multi-standard test pattern. At the same time, E5020 supports several channels: SFP and CH1 are for general-purpose, the CH2 is used for extended-purpose. SFP channel can achieve the input/output of optical signal; CH1/CH2 channel can achieve the input/output of electrical signal. Every channel has its own data input; data output and clock output (Synchronized with data output), and every channel's data and clock can turn on or turn off respectively. LCD screen shows the menu, current working mode, and test result, use the keyboard to set the working state. For convenience the test, E5020 can store up to five different working modes, which are in most common

use.

Using USB to control E5020 by PC can build up auto test system, multi-rate clock recovery, high sensitive data input (< 20mV) and optional amplitude output (50mV - 1.8V), these function are E5020's optional items.

E5020 can be used for high frequency, signal transmission performance test. As a pattern generator, it can generate multi-standard test patterns on different rate. Together with different test boards, E5020 can test BER and Eye Pattern characters of different Optical Modules such as SFP, GBIC, SFF, 1x9, and different Optical Components such as PIN-TIA, APD-TIA (Eye Pattern Analyzer or High Performance Oscilloscope is needed in Eye Pattern Test). For examples: E5020 with INSTELENT T5001 Test Board for SFP/GBIC modules test; E5020 with INSTELENT T5002 Test Board for SFF2x5, SFF2x6, SFF2x10 and 1x9 modules test; E5020 with INSTELENT T5003 Test Board for PIN-TIA and APD-TIA test.

4.2 Characteristics

Rate:

- ◆ 125Mbps、155Mbps、200Mbps、622Mbps、1.0625Gbps、1.25Gbps、1.448Gbps、2.125Gbps、2.5Gbps、2.666Gbps、3.125Gbps、4.25Gbps (Option) (Other rate, Depend on the customer's requirement)

Test wavelength:

- ◆ Multi-wavelength, from 850nm to 1610 nm (Depend on the SFP module)

Output Pattern:

- ◆ PRBS: PRBS 2^7-1 、PRBS $2^{15}-1$ 、PRBS $2^{23}-1$ and PRBS $2^{31}-1$
- ◆ K28.5: Mixed frequency test pattern for testing deterministic jitter
- ◆ CRPAT: Compliant Random Pattern
- ◆ CJTPAT: Compliant Jitter Tolerance Pattern
- ◆ Other high-frequency, low-frequency test patterns

Save mode:

- ◆ The current working mode will be saved when turned off
- ◆ Save 5 different modes, to avoid setting parameters repeatedly

SFP Channel:

- ◆ Input/Output characteristics compliant SFP Standard, reference SFP MSA
- ◆ SFP Supply Voltage(typical): $3.3V \pm 5\%$, Maximum current: 600mA, Output ripple: $< 10mV$
- ◆ SFP Clock Output: Sync with Optical Output, Amplitude: Tunable, 250mV, 450mV or 600mV

CH1 Channel:

- ◆ Input Signal Amplitude(Diff): 150mV~1600mV
- ◆ Input Impedance: Diff: 100 Ω , Single Ended: 50 Ω , AC coupled
- ◆ Output Signal Amplitude(Diff): Tunable, 500mV, 900mV or 1200mV
- ◆ Output Impedance: Diff: 100 Ω , Single Ended: 50 Ω , AC coupled
- ◆ Average Duty Cycle: $50\% \pm 5\%$
- ◆ Clock Output: Sync with Data Output, Amplitude(Diff): Tunable, 500mV, 900mV or 1200mV
- ◆ Rise/Fall Time(20%~80%): $< 100ps$
- ◆ Random Jitter: $< 4ps$, typical: 3ps
- ◆ Deterministic Jitter: $< 30ps$, typical: $< 15ps$

CH2 Channel:

- ◆ High sensitive Signal Input Channel, Input Signal Amplitude(Diff): $< 20mV \sim 1200mV$
- ◆ Input Impedance: Diff: 100 Ω , Single Ended: 50 Ω , AC coupled
- ◆ Output Signal Amplitude(Diff): 10mV~2V
- ◆ Output Impedance: Diff: 100 Ω , Single Ended: 50 Ω , AC coupled
- ◆ Average Duty Cycle: $50\% \pm 5\%$
- ◆ Clock Output: Sync with Data Output, Amplitude(Diff): Tunable, 500mV, 900mV or 1200mV
- ◆ Rise/Fall Time(20%~80%): $< 100ps$
- ◆ Random Jitter: $< 5ps$, typical: 3ps
- ◆ Deterministic Jitter: $< 50ps$, typical: $< 30ps$

USB Interface (Option):

- ◆ USB interface on the back panel, E5020 could be controlled by PC for building Auto Test System. The driver of E5020 is supplied by INSTELENT.

Keyboard:

- ◆ Keyboard on the front panel, 12 buttons to control E5020, several functions, such as, Menu Selection, Mode Set, Save, Recall, Run, Stop and so on.

LCD and Indicators:

- ◆ LCD on the front panel, the resolution is 4x20, every character is 8x6 lattice. Backlight of the LCD could be turned on/off in the menu. The Menu, Mode, and Test Result are displayed on the LCD.
- ◆ Six indicator lights on the front panel, three of them indicate on/off of CH1, CH2 and SFP respectively, other two indicate TX_FAULT and RX_LOS of SFP, and the last one indicates RUNNING.

Environmental Requirement:

- ◆ Operating Temperature: 0°C ~ +50°C
- ◆ Nonoperating Temperature: -55°C ~ +80°C
- ◆ Operating Humidity: 20% ~ 80%
- ◆ Nonoperating Humidity: 10% ~ 90%
- ◆ Power: 220V ± 20%, 50Hz ± 10%

Dimensions:

- ◆ Length: 320 mm
- ◆ Width: 297 mm
- ◆ Height: 120 mm
- ◆ Net Weight: 7 kg

5. Primary Operation

5.1 E5020's Keyboard

You can choose several testing condition on the keyboard in E5020's front panel, such as the code pattern, the channel and the rate of output. The corresponding display page on the screen is one of the following ones: the page of E5020's manufacturer information, the page of E5020's parameter

setting, the page of code pattern generating state, the page of bit error testing state, the page of save and recall. The appearance of keyboard is illustrated in the Figure 4.



Figure 4: The appearance of keyboard

Keyboard is consist of three section: general purpose keys which are indicated by red rings, save & recall key which is indicated by purple ring, functional keys which are indicated by green rings.

General-purpose keys are composed of MENU, INIT and Four direction keys.

Save & Recall key is used for save/recall the working state.

Functional keys are composed of INS, CLR, AUTO, RUN, STOP, which are used for the bit error testing.

5.2 General-purpose keys

MENU: The main menu of E5020. Three pages will show in the following order while pressing the MENU key: the page of E5020's parameter setting, the page of code pattern generating state, the page of bit error testing state. The elaborate depiction on these pages' composition and operation is arranged on the sixth chapter.

INIT: E5020 will fulfill the initialization process automatically while pressing the INIT key. The first page on screen is manufacturer's information page; the page is illustrated in the Figure 5. After two seconds, the screen will

automatically show the page of E5020's parameter setting, which is the one of the main menu pages.



Figure 5: Information of Manufacture

Four direction keys: up and down key are used for choosing the proper row in a page. Left and right key are used for choosing the different parameter.

5.3 Save & Recall key

The SAVE & RECALL key can store up to five state of parameter setting, which is frequently used. So, you can recall the required state directly using the key and avoid the parameter setting process. The appearance of this page is illustrated in the Figure 6.

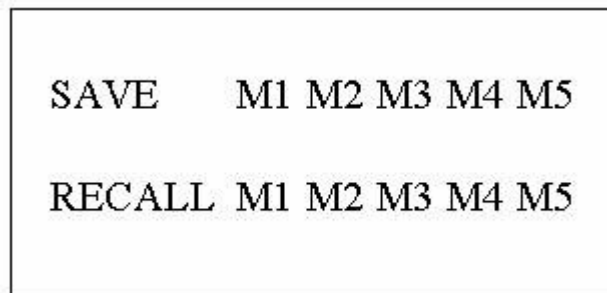


Figure 6: Save & Recall page

The following steps are about save & recall function.

First, set the required parameter state in the page of E5020's parameter setting. The elaborate depiction on the setting process is arranged in the sixth chapter.

Second, you finish the parameter setting and then go to the page of code pattern generating state and the page of bit error testing state to check the setting.

Third, after affirming the settings and pressing the SAVE RECALL key, the screen will show the page illustrated as Figure 6. Using the ascending and descending key to choose the row of SAVE, then using the left and right key to choose the name of stored mode (M1/M2/M3/M4/M5).

How to recall a state which was stored before? The following steps will tell you.

First, press the SAVE RECALL key and go to the save & recall page.

Second, use the ascending and descending key to choose the RECALL row.

Third, use the left and right key to choose a settings mode (M1/M2/M3/M4/M5), which would be your required one, then press the SAVE RECALL key to enter the state.

Note 1: Eight kinds of parameter except BACKLIGHT can be saved.

Note 2: The settings about *OUTPUT VOLTAGE AMPLITUDE* and *SERIAL INTERFACE BAUD RATE* are not shown in the page of code pattern generating state and the page of bit error testing state.

5.4 Functional keys

The INS key, CLR key, AUTO key, RUN key and STOP key are valid during the bit error test, their function and operation are described in the sixth chapter.

6. Page settings and screen display

When pressing the MENU key, screen will display the following pages in order. The sequence of them is *Parameter settings page of E5020*→*Code pattern generating state page of E5020*→*Bit error test state page of E5020*. The pages composition and settings will be introduced in turn.

6.1 Parameter settings page of E5020

In this page, you can set nine kinds of parameters, which are narrated in the screen displaying order. And “/” indicates that choose a parameter settings through left and right key.

1. Code pattern: It is located in the first row, and display as follows:

PATTERN:

PRBS $2^7 - 1/2^{15} - 1/2^{23} - 1/2^{31} - 1/K28.5/*K28.7/*D21.5*/CJTPAT/CRPAT$

2. Data rate: It is located in the second row, and display as follows:

DATA RATE:

125M/155M/200M/622M/1.0625G/1.25G/1.448G/2.125G/2.5G/2.666G

/3.125G

3. CH1 output state: It is indicated the state of data and clock output from channel 1. Located in third and fourth row, and display as follows:

CH1 DOUT→ON/OFF

CH1 COUT→ON/OFF

4. CH2 output state: It is indicated the state of data and clock output from channel 2. Located in fifth and sixth row, and display as follows:

CH2 DOUT→ON/OFF
CH2 COUT→ON/OFF

5. SFP output state: It is indicated the state of data and clock output from channel 2. Located in seventh and eighth row, and display as follows:

SFP DOUT→ON/OFF
SFP COUT→ON/OFF

NOTE: Choosing either of Data and clock output from CH1, CH2, SFP and setting its state as ON, the corresponding channel indicator lamp which lies in the left of keyboard will be lighted to facilitate the test process.

6. Output voltage amplitude: It is located in the ninth row, and display as follows:

AMPLITUDE→500mV/900mV/1200mV

7. BERT channel: It is located in the tenth and eleventh row, and display as follows:

BERT FROM→CH1/CH2/SFP
BERT TO→CH1/CH2/SFP

8. Screen backlight: It is located in the twelfth row, and display as follows:

BACKLIGHT→ON/OFF

9. Serial interface baud rate: It is located in the thirteenth row, and display as follows:

BAUD RATE→4800/9600/19200/57600/115200

6.2 Code pattern generating state page of E5020

In the Parameter settings page of E5020, when you press MENU key, then you will go to the code pattern generating state page of E5020. There are the statistical results about the parameter settings, which are set in parameter settings page. Figure 7 illustrates the appearance of this page.

```

GEN→code pattern Data rate
CH1→DOUT:state CLK: state
CH2→DOUT:state CLK: state
SFP →DOUT:state CLK: state

```

Figure 7: Code pattern generating state page

6.3 Bit error test state page of E5020

When testing the bit error performance, the recommendable code patterns are PRBS $2^7 - 1$, PRBS $2^{15} - 1$ and PRBS $2^{23} - 1$. Other patterns are not recommended.

1. The appearance of page

In this page, pressing the MENU key, you will go to the page of bit error testing state, which is the state show of the current testing. Figure 8 illustrates this page.

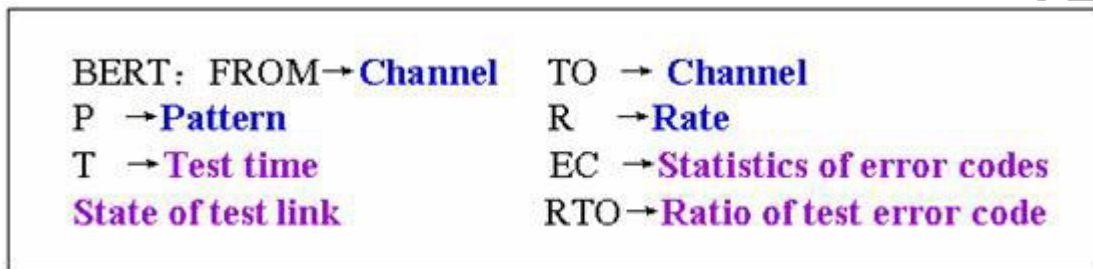


Figure 8: BER test state page

Note: The colorful words in the Figure 8 are not the real appearance of this page, only for the convenience of the following narration.

The blue words show the current states of the parameters. That is to say, when you finish the parameters setting in the current test, these blue words are settled.

The purple words are the real-time statistic results of the current test. In other words, these purple words are varied with the current test.

Additionally, the state of test link in this page is manifest at a glance of the link status under test. This item reveals adequately that E5020 is intelligent and user-friendly equipment; you can infer the status of test link as long as you have knowledge of every kind of meanings of this item. So, remember these state by heart will give facilities for your test.

There are four kinds of state in this item: NO SIG, SYN..., SYN OK and STOP.

E5020 detects that the test link is break off, NO SIG will be employed.

After detecting that the link is under connection, E5020 will perform automatically the process of synchronization. The item will present SYN... sparkingly during this process, the interval of time is approximate 0.4 second.

After finishing the link synchronization, the item will present SYN OK sparkingly; the interval of time is approximate 1 second. At the same time, the purple words section will start the results statistic of the bit error test.

When pressing the STOP key, the item will present STOP and reveal that the current test is cease. If you press the AUTO or RUN key, the test will be start

again.

2. The functional-key in bit error test

AUTO: Auto bit error test key. When the status of test link is bad, usually because the link is break off. Once you press the AUTO key, E5020 will perform synchronization process intelligently as it happens, then start a new test of bit error. That is to say, the test time, the statistic of bit errors and the ratio of bit error will start a fresh. We recommend especially the AUTO key to use in a successive and quick test of many components' or modules' bit error performance.

RUN: Manual bit error test key. When the status of test link is bad, usually because the link is break off. Once you press the RUN key, E5020 will perform synchronization process intelligently as it happens, then continue the test of bit error. That is to say, the test time, the statistic of bit errors and the ratio of bit errors will be added to the previous test results. We recommend especially the RUN key to use in a continuous test of single component or module's bit error performance.

INS: E5020 will insert one error bit in the current test and the EC item will add 1 while pressing the INS key. Using this key, you can inspect conveniently the performance of error spread in your test.

CLR: Clear the bit errors in current test. The EC item will be set to zero when pressing the key.

STOP: Stop the current test. The link status item will be set to STOP when pressing the key.

7. Appendix

7.1 Introduction of PRBS code pattern

The PRBS $2^7 - 1$, PRBS $2^{15} - 1$, PRBS $2^{23} - 1$ and PRBS $2^{31} - 1$ pattern generated by E5020 are conformed to the standard definition of ITU-T. The related documents defining the PRBS code pattern are O.150 and O.151. Table1 shows the application field of the different PRBS code pattern.

Code pattern	Polynomial	Recommendatory application field
PRBS $2^7 - 1$	$2^7 + 2^6 + 1$	Test modules & components applied in Ethernet and ATM
PRBS $2^{15} - 1$	$2^{15} + 2^{14} + 1$	By user's requirement
PRBS $2^{23} - 1$	$2^{23} + 2^{18} + 1$	Test modules & components applied in SDH and SONET
PRBS $2^{31} - 1$	$2^{31} + 2^{28} + 1$	By user's requirement

Table 1: PRBS code pattern

To explain the PRBS code pattern's generation, take example for PRBS $2^{15}-1$ code pattern. The sequence may be generated in a fifteen-stage shift register whose 14th and 15th stage outputs are added in a modulo-two addition stage and the result is fed back to the input of the first stage.

7.2 Introduction of the CRPAT and CJTPAT code pattern

The Fiber Channel working group submitted a Working Draft for Methodologies for Jitter Specifications (MJS) in 1998. This draft was a technical report to the Accredited Standards Committee of National Committee for Information Technology Standardization (NCITS) and has a revision number known as T11.2/Project 1230/Rev 7, December 16, 1998.

The MJS document defined several jitter test patterns. The RPAT (Random Pattern) was developed to provide a broad and flat spectral content of frequency; a modified version of this was also defined in which the format of the pattern was properly encapsulated within a "compliant" frame structure, and is named CRPAT (Compliant Random Pattern). The CJTPAT (Compliant Jitter Tolerance Pattern) was developed to provide a data stream which would induce large instantaneous phase jumps; a modified version of this was also defined in which the format of the pattern was properly encapsulated within a "compliant" frame structure, and is named CJTPAT (Compliant Jitter Test Pattern).

The following tables describe the sequential bit sequence of the CRPAT and CJTPAT patterns. The tables are arranged such that the time domain occurrence of the bits is from left to right, and top to bottom. The tables are divided into groups of three rows, which contain the information show in Table 2.

Code group name (octet value) row								
10B code group sequence row								
BERT hex row								

Table2: CRPAT and CJTPAT code patterns' format

Code Group Name (Octet Value): This row lists the code groups transmitted in time domain order (from left to right, top to bottom). The Octet value (8-bit HEX prior to 8B10B encoding) of the code group is listed in parenthesis.

10B Code Group Sequence: This row lists the individual bit sequence in the pattern in time domain order (from left to right, top to bottom). The 10-bit code groups are broken into 4-bit sequences for the convenience of programming Bit Error Rate Test (BERT) receivers; the 4-bit fields allow you to better fit the 10B data sequence into such byte-oriented equipment.

BERT Hex: The majority of BERT instruments use 8-bit bytes for programming long data patterns. Be aware that BERT equipment generally transmits (and

expects at the paired BERT receiver) the least significant bit (LSB) first and the most significant bit (MSB) last. BERT equipment is programmed, though, in the Octet Hex manner in which the most significant hex value is listed first and least significant hex value last (that is, a hex value of F0 would be transmitted in a bit sequence of 00001111). For the your convenience, the 4-bit sequences of the middle row are grouped into 8-bit bytes in the third bottom row and the BERT hex value to match the LSB-first, MSB-last sequence is listed.

Table3 shows the CRPAT code pattern sequence.

Idle Primitive (Repeated 6 times)									
K28.5 (BC)		D21.4 (95)			D21.5 (B5)			D21.5 (B5)	
0011	1110	1010	1010	0010	1010	1010	1010	1010	1010
7C		55			54			55	
Start PF Frame (Class 3 normal: SOFn3)									
K28.5 (BC)		D21.5 (B5)			D22.1 (36)			D22.1 (36)	
0011	1110	1010	1010	1010	0110	1010	0101	1010	1001
7C		55			65			A5	
RPAT Sequence (Repeated 16 times)									
D30.5 (BE)		D23.6 (D7)			D3.1 (23)			D7.2 (47)	
1000	0110	1011	1010	0110	1100	0110	0100	0111	0101
61		5D			36			26	
D11.3 (6B)		D15.4 (8F)			D19.5 (B3)			D20.0 (14)	
1101	0000	1110	1000	1101	1100	1010	1000	1011	0100
0B		17			3B			15	
D30.2 (5E)		D27.7 (FB)			D21.1 (35)			D25.2 (59)	
0111	1001	0100	1001	1110	1010	1010	0110	0110	0101
9E		92			57			65	
Cyclic Redundancy Check (CRC)									
D14.7 (EE)		D3.1 (23)			D21.2 (55)			D22.0 (16)	
0111	0010	0011	0001	1001	1010	1001	0101	1010	1011
4E		8C			59			A9	
End of Frame (Pattern dependent EOFn)									
K28.5 (BC)		D21.5 (B5)			D21.6 (D5)			D21.6 (D5)	
1100	0001	0110	1010	1010	1010	1001	1010	1010	0110
83		56			55			59	

Table3: The CRPAT code pattern sequence

Table4 shows the CRJPAT code pattern sequence.

Idle Primitive (Repeated 6 times)										
K28.5 (BC)			D21.4 (95)			D21.5 (B5)			D21.5 (B5)	
0011	1110	1010	1010	0010	1010	1010	1010	1010	1010	
7C		55		54		55		55		
Start of Frame (Class 3 normal: SOFn3)										
K28.5 (BC)			D21.5 (B5)			D22.1 (36)			D22.1 (36)	
0011	1110	1010	1010	1010	0110	1010	0101	1010	1001	
7C		55		65		A5		95		
Low Density Transition Pattern (Repeated 41 times)										
D30.3 (7E)			D30.3 (7E)			D30.3 (7E)			D30.3 (7E)	
1000	0111	0001	1110	0011	1000	0111	0001	1110	0011	
E1		78		1C		8E		C7		
Transferring from Low to High Transition Densities										
D30.3 (7E)			D30.3 (7E)			D30.3 (7E)			D20.3 (74)	
1000	0111	0001	1110	0011	1000	0111	0000	1011	1100	
E1		78		1C		0E		3D		
D30.3 (7E)			D11.5 (AB)			D21.5 (B5)			D21.5 (B5)	
0111	1000	1111	0100	1010	1010	1010	1010	1010	1010	
1E		2F		55		55		55		
HIGH Density Transition Pattern (Repeated 12 times)										
D21.5 (B5)			D21.5 (B5)			D21.5 (B5)			D21.5 (B5)	
1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
55		55		55		55		55		
Transferring from High to Low Transition Densities										
D21.5 (B5)			D30.2 (5E)			D10.2 (4A)			D30.3 (7E)	
1010	1010	1010	0001	0101	0101	0101	0101	1110	0011	
55		85		AA		AA		C7		
D30.3 (7E)			D30.3 (7E)			D30.3 (7E)			D30.7 (FE)	
1000	0111	0001	1110	0011	1000	0111	0001	1110	0001	
E1		78		1C		8E		87		
Cyclic Redundancy Check (CRC)										
D21.7 (F5)			D14.1 (2E)			D22.7 (F6)			D29.6 (DD)	
1010	1011	1001	1100	1001	0110	1000	0110	1110	0110	
D5		39		69		61		67		
End Of Frame (Pattern dependent EOFn)										
K28.5 (BC)			D21.5 (B5)			D21.6 (D5)			D21.6 (D5)	
1100	0001	0110	1010	1010	1010	1001	1010	1010	0110	
83		56		55		59		65		

Table4: The CJTPAT code pattern sequence

7.3 Recover the clock from external signals (Extended)

1. Recover clock and data from external optical signals

It is easy to accomplish the clock and data recovery from external optical signals using E5020. The recommendatory method is illustrated in Figure9.

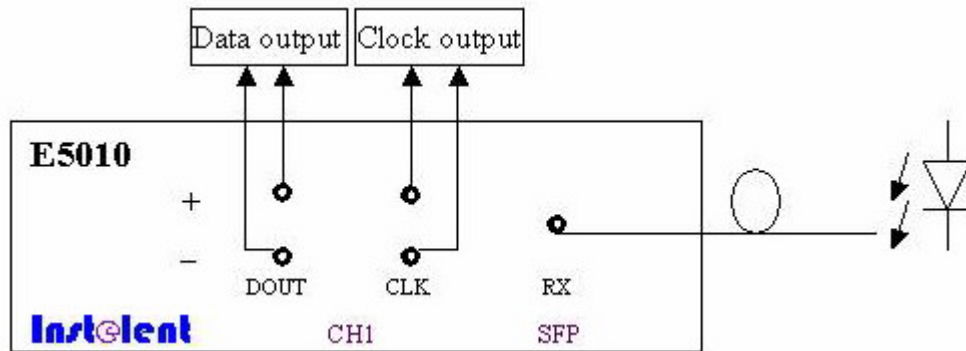


Figure 9: Recovery from external optical signal

E5020 receive the external optical signals through the SFP Rx interface, which transmit the optical signals into the corresponding electrical signals. They will experience the recovery circuit inside the E5020, and the required signals will output separately from DOUT and CLK of CH1.

Note: SFP's receive wavelength should satisfy the external optical signals. The data rate of SFP should be set to the optical signals' rate.

2. Recover clock and data from external electrical signals

It is easy to accomplish the clock and data recovery from external electrical signals using E5020. The recommendatory method is illustrated in Figure10.

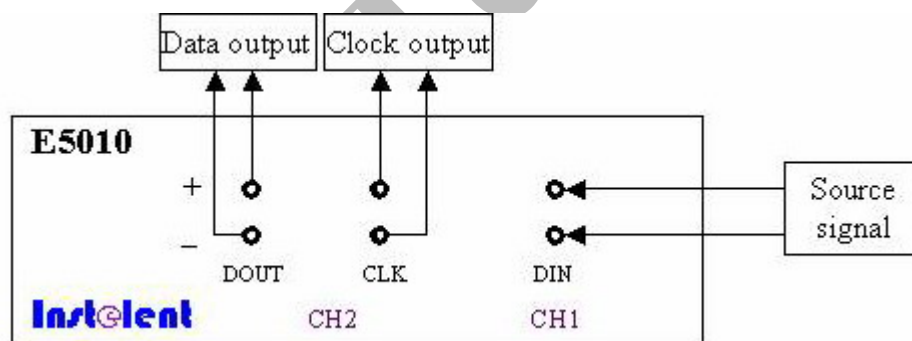


Figure 10: Recovery from external electrical signal

E5020 receive the external electrical signals through the CH1 DIN interface, which transmit the electrical signals to the recovery circuit inside the E5020, and the required signals will output separately from DOUT and CLK of CH2.

Note: CH1's receive data rate should be equal to the external electrical signals.

8. Common glossary in optical communication test

Accuracy: The closeness of the indicated value to the true value.

Attenuation: A decrease in magnitude of current, voltage, or power of a signal.

Attenuator: A transducer that reduces the amplitude of a signal.

Bandwidth: The difference between the high and low frequencies of a transmission band.

BER: An acronym for Bit Error Ratio (or Rate), which is the principal measure of quality of a digital transmission system. BER is defined as: $BER = \text{Number of Errors} / \text{Total Number of Bits}$.

BER Floor: A limiting of the bit-error-ratio in a digital system as a function of received power due to the presence of signal degradation mechanisms or noise.

Bit Error: An incorrect bit. Also known as a coding violation.

Bit Rate: The number of bits transmitted in a specified (usually 1 second) time.

Channel: A communications path or the signal sent over a channel.

Channel capacity: The maximum usable data rate for a given channel.

Clock: A signal that provides a timing reference.

Clock recovery: Recovering the clock from the incoming data.

dB: Decibel: a method of expressing power or voltage ratios. The decibel scale is logarithmic.

dBm: The symbol for power level in decibels relative to 1 mW.

Deterministic jitter: The difference between the maximum and minimum deviations from the expected timing positions of data after removing the random jitter.

Differential (relating to data (electrical) signal): A signal transmission method that requires the voltage levels in a pair of cables/signals to convey information.

Digital Signal: A signal made up of a series of on and off pulses.

Digital Transmission System: A transmission system where information is transmitted in a series of on and off pulses.

Dispersion (example in fiber): In an optical system, the broadening and distortion of a pulse due to multi-path waveform propagation.

Fiber optics: A method of transmitting information in which light is modulated and transmitted over high-purity, filaments of glass. The bandwidth of fiber optic cable is much greater than that of copper wire.

Fiber Optics Transmission System (FOTS): A transmission system transmitting light through thin glass fibers.

GBIC: Gigabit interface converter modules are transceivers that complete a

link. GBICs are available in short and long wavelength optical and in metallic twisted pair cable designs.

SFF: An acronym for Small Form Factor.

SFP: An acronym for Small Form factor Pluggable.

Link: A transmission path between two stations, channels, or parts of a system.

LOS: An acronym for Loss of Signal.

Long wavelength: The spectrum from 1200 to 1600 nanometers.

Short wavelength: The spectrum from 800 to 1000 nanometers.

PRBS: Pseudo-random binary-pulse sequence. A repeating bit pattern that appears to be random. The bit pattern is used for telecommunications system testing.

Random jitter: Jitter whose value at a future instant cannot be predicted.

Rx: An abbreviation for receiver.

Tx: An abbreviation for transmitter

Terminal: A point where information enters or leaves a communications network. An input or output device designed to send or receive data.

9. Index of terms in E5020 (As sequence of alphabet)

AMPLITUDE: The amplitude of voltage, the units is millivolt.

AUTO: The auto key of bit error test.

BACKLIGHT: The item is used for opens or closes the backlight function of screen.

BAUD RATE: The baud rate of E5020's serial interface.

BERT: The test of bit error ratio. In E5020's page of parameter settings, BERT FROM CH1/CH2/SFP expresses that input channel of the BERT is CH1/CH2/SFP accordingly. BERT TO CH1/CH2/SFP expresses that output channel of the BERT is CH1/CH2/SFP accordingly. (The "/" denotes that you can choose the parameter through the left and right key.)

CH1: The channel 1.

CH2: The channel 2.

CJTPAT: An acronym for Compliant Jitter Tolerance Pattern.

CLK: The path of clock signal.

CLR: In the BERT, the key is used for clear the error bit and set zero to the error counter.

COUT: The output of clock signal.

CRPAT: An acronym for Compliant Random Pattern.

DATA RATE: The rate of data.

DIN: The input of data.

DOUT: The output of data.

***D21.5*:** A test pattern of high frequency.

EC: The counter of error bit.

GEN: The generating pattern of E5020.

INIT: The key is used for start the initial process of E5020.

INS: In the BERT, the key is used for insert a error bit to the current test.

K28.5: A test pattern is used to the mixed frequency and deterministic jitter test.

***K28.7*:** A pattern is characteristic for the quarter of rate.

Mx: The mode of save & recall is **x**.

MENU: The key is used for show the menu of E5020.

NO SIG: The item denotes that the link status is too bad and cannot receive signal.

ON/OFF: Open or close a function.

PATTERN: The pattern kind generates from E5020.

P: An acronym for pattern.

PRBS: An acronym for pseudo-random binary-pulse sequence. E5020 can generate the following four kinds of PRBS: $PRBS 2^7 - 1$, $PRBS 2^{15} - 1$, $PRBS 2^{23} - 1$ and $PRBS 2^{31} - 1$.

R: An acronym for rate.

RECALL: In save & recall page, choosing this item to resume a saved test state.

SAVE: In save & recall page, choosing this item to store a test state.

SAVE RECALL: Using the key to enter the save & recall page.

SFP: The interface of SFP in E5020.

STOP: In the BERT, the key is used for stop the current test.

SYN...: The item denotes that E5020 is under synchronization automatically.

SYN OK: The item denotes that E5020 has achieved the synchronization process.

T: The timer of current test.

+: The in-phase end of differential input or output.

-: The reverse-phase end of differential input or output.

10. After Sale Service

In the first year after you have purchased E5020, only the damnification caused by instrument's quality problem can return INSTELENT for free service, any damnification caused by man-made factor also can return INSTELENT for repair but charge solely.

Note: If you have any question, please contact INSTELENT.

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