EOLC-161HG-S-10-L1A Series

Single-Mode OTU4 4I1-9D1F CFP4 Transceiver
Single-Mode 100GBASE-LR4 CFP4 Transceiver
RoHS6 Compliant

Features

- Supports 103Gbps and 112Gbps aggregate bit rates
- Single 3.3V Power Supply and Power dissipation < 6W
- Up to 10km transmission on SMF
- Hot-Pluggable CFP4 Footprint Duplex LC Connector Interface
- Class 1 FDA and IEC60825-1 Laser Safety Compliant
- RoHS6 Compliant
- Operating Case Temperature
  Standard: 0℃~+70℃
- Compliant with CFP4 MSA Specification
- MDIO interface with integrated Digital Diagnostic Monitoring
- No external reference clock

Applications

- 100GBASE-LR4 Ethernet
- OTU4 4I1-9D1F

Ordering Information

Part No.	Data Rate*note2	Distance*note1	Interface	Temp.	DDMI
EOLC-161HG-S-10-L1A	103.125Gbps /111.81Gbps	10km	LC	Standard	Yes

Note1: 9/125μm SMF
Note2: Switching between 100GBASE-LR4 and OTU4 4I1-9D1F through MDIO.

*The product image only for reference purpose.

Regulatory Compliance*

Product Certificate	Certificate Number	Applicable Standard
TUV	R50135086	EN 60950-1:2006+A11+A1+A12+A2
		EN 60825-1:2014
		EN 60825-2:2004+A1+A2
UL	E317337	UL 60950-1
		CSA C22.2 No. 60950-1-07
EMC CE	AE 50285865 0001	EN 55022:2010
		EN 55024:2010
FCC	WTF14F0514417E	47 CFR PART 15 OCT., 2013
FDA	/	CDRH 1040.10
ROHS	/	2011/65/EU

*The above certificate number updated to June 2014, because some certificate will be updated every year, such as FDA and ROHS. For the latest certification information, please check with Eoptolink.

Absolute Maximum Ratings*note3

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%
ESD*note4			500	V

Note3: Exceeding any one of these values may destroy the device immediately.
Note4: Human body model.

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T_C		0		70	°C
Power Supply Voltage	Vcc		3.2	3.3	3.4	V
Power Supply Noise	DC-1MHz			2		%
	1-10MHz			3		
Power Consumption	P	MAX			6	W
		Low Power Mode			1	
Time of Power-On sequence & Reset Sequence				TBD		sec
Modulation Format				NRZ, Mark Ratio 50%		

Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Input Amplitude (Differential)	Vin	150		1000	mVpp	AC coupled inputs*(Note7)

Input Impedance (Differential)	Zin	85	100	115	ohms	Rin > 100 kohms @ DC
Receiver						
Output Amplitude (Differential)	Vout	360		900	mVpp	AC coupled outputs*(Note7)
Output Impedance (Differential)	Zout	85	100	115	ohms	
Output Rise/Fall Time	t_r/t_f	9.5			ps	20%~80%

1.2V MDIO Interface Specifications

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Input Voltage	V_{IH}	0.84		1.5	V	
	V_{IL}	-0.3		0.36	V	
Input Leak current	I_{IN}	-100		100	uA	
Output Voltage	V_{OH}	1.0		1.5	V	
	V_{OL}	-0.3		0.2	V	
Input Capacitance	C_I			10	pF	
Input MDC Clock	f_{MDC}	0.1		4	MHz	
MDC Clock Period	T_{MDC}	250		10000	ns	
MDIO Hold Time	T_{hold}	10			ns	
MDIO SetupTime	T_{setup}	10			ns	
Clock to output delay from the MMD	T_{dely}	0		300	ns	
GLB_ALM	$T_{glb\_alm\_ass}$			150	ms	
	$T_{glb\_alm\_dea}$			150	ms	
MDC High time	T_{high}			160	ns	
MDC Low time	T_{low}			160	ns	

Optical and Electrical Characteristics

OTU4 4I1-9D1F Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		27.95		Gbps
Data Rate Variation		-20		+20	ppm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Total Average Output Power*(Note5)	Po			8.9	dBm
Average Launch Power per Lane	Peach	-2.5		2.9	dBm
Maximum channel power difference				5	dB
Channel spacing			800		GHz
Maximum spectral excursion		-184		184	GHz

Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Extinction Ratio*(Note6)	ER	7			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note6)		G.959.1 Compliant			
TX Disable Assert Time	t_off			100	us
Receiver					
Signaling Speed per Lane	BR_{AVE}		27.95		Gbps
Data Rate Variation		-20		+20	ppm
Damage threshold	Rdam	5.5			dBm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane	Rpow	-8.8		2.9	dBm
Equivalent Receive Sensitivity per Lane*(Note8)	Pmin			-10.3	dBm
Maximum channel power difference				5.5	dB
Maximum optical path penalty				1.5	dB
Optical Return Loss	ORL			-26	dB
LOS Assert	LOSA	-21.3			dBm
LOS De-Assert	LOSD			-11.3	dBm
LOS Hysteresis		0.5			dB

100GBASE-LR4 Operation

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Total Average Output Power*(Note5)	Po			10.5	dBm
Average Launch Power per Lane	Peach	-4.3		4.5	dBm
Difference in launch power between any two lanes				5	dB
Average launch power of OFF transmitter per lane				-30	dBm
Optical Return Loss Tolerance				20	dB
Transmitter reflectance				-12	dB
Extinction Ratio*(Note10)	ER	4			dB
Transmitter eye mask definition {X1,		IEEE 802.3 Clause 88 100Gbase-LR4			

X2, X3, Y1, Y2, Y3}*(Note10)		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
TX Disable Assert Time	t_off			100	us
Receiver					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold	Rdam	5.5			dBm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane	Rpow	-10.6		4.5	dBm
Receive Sensitivity in OMA per Lane*(Note12)	Pmin			-8.6	dBm
Stressed Sensitivity(OMA) per lane	SRS			-6.8	dBm
Optical Return Loss*(Note11)	ORL			-26	dB
LOS Assert	LOSA	-20.6			dBm
LOS De-Assert	LOSD			-10.6	dBm
LOS Hysteresis*(Note 9)		0.5			dB

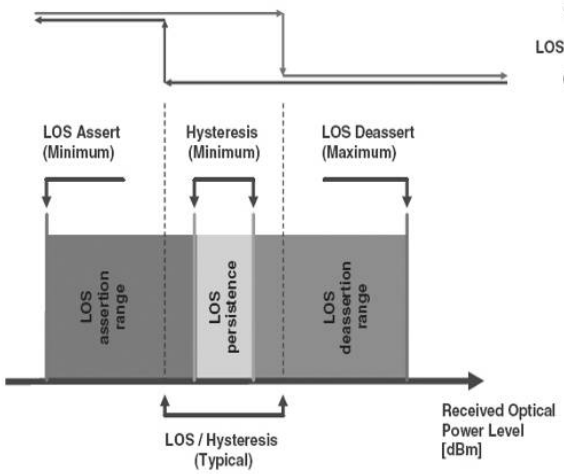
Note5: Output is coupled into a 9/125μm single-mode fiber.

Note6: Filtered, measured with a PRBS 2^{31}-1 test pattern @27.95Gbps

Note7: High speed I/O, internally AC coupled.

Note8: Minimum average optical power measured at BER less than 1E-5, with a 2^{31}-1 PRBS without FEC. The maximum bit error ratio for this application of 1E-12 is only after error correction has been applied.

Note 9: LOS Hysteresis



Note10: Filtered, measured with a PRBS 2^{31}-1 test pattern @25.78Gbps

Note11: Conditions of stressed receiver sensitivity test at 1.8 dB vertical eye closure penalty per lane, 0.2 UI stressed eye J2 Jitter per lane, 0.47UI stressed eye J9 Jitter per lane.

MDIO Registers for Signal Rate Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	3:1	Tx Rate Select	000b: GBE 25.8G (Initial Value) 011b: OTU4 28G	Note13
A012h	R/W	3:1	RX Rate Select	000b: GBE 25.8G (Initial Value) 011b: OTU4 28G	Note13

Note13: Written with unsupported data rate will have no effect to the CFP4 module.

MDIO Registers for MCLK

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	7:5	TX MCLK Control	000b: Disabled (Initial Value) 010b: 1/8 of network lane	
A012h	R/W	7:5	RX MCLK Control	000b: Disabled (Initial Value) 010b: 1/8 of network lane	
A015h	R/W	13:12	MCLK Selection	Selects the source of the MCLK for CFP4 modules. 00b: MCLK Off (Initial Value). 01b: MCLK = TX_MCLK 10b: Reserved. 11b: Reserved.	

MDIO Registers for Host Lane Control Controls Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A440~A443h	R/W	15	Signal equalization mode control	0: Automatic (Initial Value) 1: Manual	
	R/W	12~9	Signal Equalization Gain	00h: No EQ (Initial Value). Write 9~0 to set 9 ~ 0 Db of gain in manual mode.	
	R/W	3~0	Rx Signal Pre/ De-emphasis	0000b: 0Db (Initial Value). 4-bit unsigned number N represents the pre/de-emphasis applied. Pre/De-emphasis = 0.5 Db * N, N = 0, 15.	

MDIO Registers for Host Lane RX Squelch Mode Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A014h	R/W	9	Automatic Host Lane Output Squelch on LOS	0: Host Lane shall not squelch Rx RF output on RX_LOS. Host controls squelch using A040h (Initial Value). 1: Host Lane shall squelch Rx RF output on RX_LOS (sync with A210h~A21Fh.4) per lane based.	
A040h	R/W	15~0	Host Lane Output Squelch Control	Bits 15~0 squelches host lane 15~0 Rx RF output respectively. 0: No squelch(Initial Value). 1: Squelch.	

MDIO Registers for Network Lane Squelch & Disable Selection

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	15	Automatic Network Lane TX Squelch Mode	0: Network Lane shall squelch TX Average power on TX_LOL (sync with A210h~A21Fh.6) per lane base (Initial Value). 1: Network Lane shall squelch TX OMA power on TX_LOL (sync with A210h~A21Fh.6) per lane base.	
	R/W	4	Automatic Network Lane TX Squelch Control	0: Network lane automatic control on TX_LOL is off. Host controls each lane TX squelch using A041h (Initial Value). 1: Network lane automatic control on TX_LOL is on per lane base.	
A013h	R/W	15~0	Lane 15~0 Disable	Bits 15~0 disable network lane 15~0 Tx Average power output respectively. 0: Normal(Initial Value). 1: Disable.	
A041h	R/W	15~0	Network Lane n TX Squelch	Bits 15~0 squelches network lane 15~0 Tx OMA power output respectively. 0: No squelch(Initial Value). 1: Squelch.	

MDIO Registers for TX/Rx Reset

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A011h	R/W	8	TX Reset	0: Normal operation(Initial Value), 1: Reset.	Note15
A012h	R/W	8	RX Reset	0: Normal operation(Initial Value), 1: Reset.	Note15

Note15: Set these registers to 1 will keep the correspond CDR in reset sate. While these bits are cleared, the correspond CDR will be re-initialized.

MDIO Registers for PRG_CNTL1/Tx_DIS

MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A007h	R/W	7~0	Function Select Code	0: Assert/De-Assert of PRG_CNTL1 has no effect. 0x01: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 =Assert (Reset). 2~9: MSA reserved. 0x0A: TX_DIS (Initial Value).	Note14

Note14: CFP4 module multiplexes PRG_CNTL1 with TX_DIS functions. Host shall use this register to assign

TX_DIS function to PRG_CNTL1,if and only if module is in Low_Power State. When A007h is set to 0x01 in low power state, then the TRXIC_RSTn function is enabled and the hardware TX_DIS is assigned to be deasserted.

MDIO Registers for PRG_ALRM1

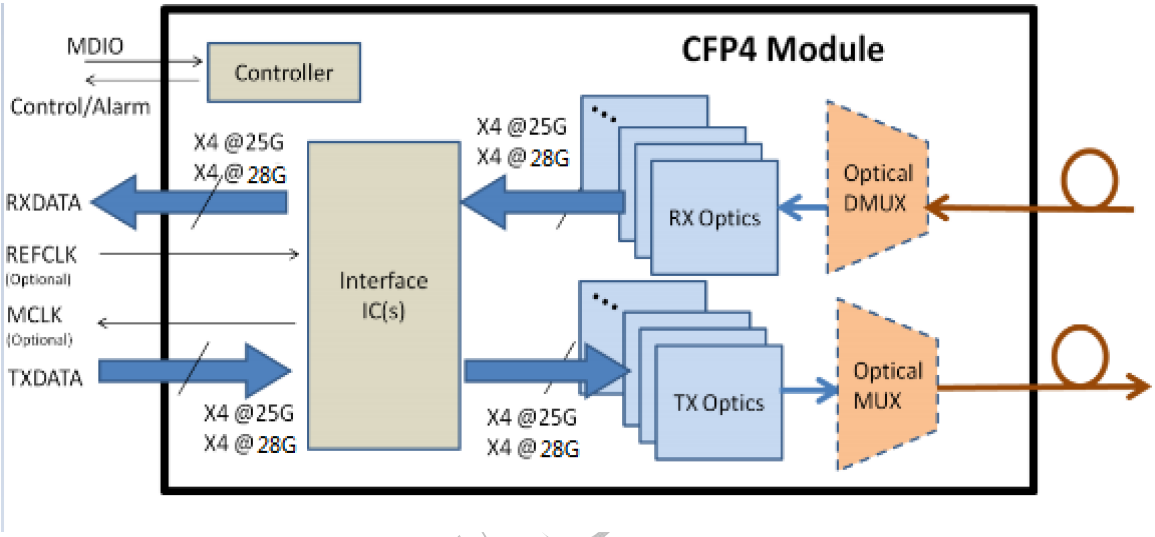
MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A00Ah	R/W	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, 10: RX_LOS(Initial Value). 11~255: Reserved.	

MDIO Registers for RX Power Monitor Alarm/Warning Threshold

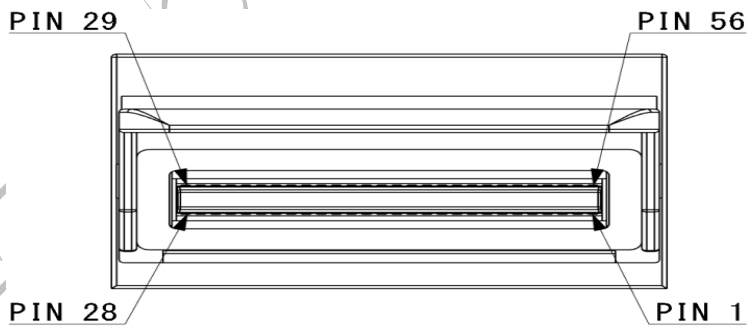
MDIO Hex Addr	Access Type	Bit	Register Name	Value and Description	Notes
A015h	R/W	9	RX Power Monitor Alarm/Warning Threshold Select	0: MSA default registers 80C0h~80C7h (Initial Value), 1: Host Configured Receive Optical Power Threshold registers A03Ch~A03Fh..	Note15
A03Ch	R/W	15~0	Host Configured Receive Optical Power High Alarm Threshold	Valid if the value is between “Host Configured Receive Optical Power High Alarm Permissible Minimum Threshold” (80E8h) and “Host Configured Receive Optical Power High Alarm Permissible Maximum Threshold” (80F0h). Value beyond the threshold shall generate no effect.	
A03Dh	R/W	15~0	Host Configured Receive Optical Power High Warning Threshold	Valid if the value is between “Host Configured Optical Power High Warning Permissible Minimum Threshold” (0x80EA) and “Host Configured Optical Power High Warning Permissible Maximum Threshold” (80F2h). Value beyond the threshold shall generate no effect.	
A03Eh	R/W	15~0	Host Configured Receive Optical Power Low Warning Threshold	Valid if the value is between “Host Configured Optical Power Low Warning Permissible Minimum Threshold” (80Ech) and “Host Configured Optical Power Low Warning Permissible Maximum Threshold” (80F4h). Value	

				beyond the threshold shall generate no effect.	
A03Fh	R/W	15~0	Host Configured Receive Optical Power Low Alarm Threshold	Valid if the value is between “Host Configured Receive Optical Power Low Alarm Permissible Minimum Threshold” (80Eeh) and “Host Configured Receive Optical Power Low Alarm Permissible Maximum Threshold” (80F6h). Value beyond the threshold shall generate no effect.	

Functional Description of Transceiver



CFP4 Transceiver Electrical Pad Layout



Pin Function Definitions

CFP4	
Top	
56	GND
55	TX3n
54	TX3p
53	GND
52	TX2n
51	TX2p
50	GND

CFP4	
Bottom	
1	3.3V_GND
2	3.3V_GND
3	3.3V
4	3.3V
5	3.3V
6	3.3V
7	3.3V_GND

49	TX1n
48	TX1p
47	GND
46	TX0n
45	TX0p
44	GND
43	*(REFCLKn)*
42	*(REFCLKp)*
41	GND
40	RX3n
39	RX3p
38	GND
37	RX2n
36	RX2p
35	GND
34	RX1n
33	RX1p
32	GND
31	RX0n
30	RX0p
29	GND

8	3.3V_GND
9	VND_IO_A
10	VND_IO_A
11	TX_DIS (PNG_CNTL1)
12	TX_LOS (PNG_ALRM1)
13	GLB_ALRMn
14	MOD_LOPWR
15	MOD_ABS
16	MOD_RSTn
17	MDC
18	MDIO
19	PRTADR0
20	PRTADR1
21	PRTADR2
22	VND_IO_C
23	VND_IO_D
24	VND_IO_E
25	GND
26	*(MCLKn)*
27	*(MCLKp)*
28	GND

Bottom Row Pin Descriptions

Pin Num.	Name	Function	Notes
1	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
2	3.3V_GND		
3	3.3V	3.3V Module Supply Voltage	3.3V ± 5%
4	3.3V		
5	3.3V		
6	3.3V		
7	3.3V_GND	Ground	3.3V Module Supply Ground, Internally connected to Signal Ground
8	3.3V_GND		
9	VND_IO_A	I/O	Module Vendor I/O A. NC
10	VND_IO_B	I/O	Module Vendor I/O B, NC
11	TX_DIS (PNG_CNTL1)	I	“1” or NC = transmitter disabled, “0” = transmitter enabled
12	TX_LOS (PNG_ALRM1)	O	“1” = loss of signal (low optical signal), “0” = normal condition
13	GLB_ALRMn	O	“0” = alarm condition in any MDIO Alarm register, “1” = no alarm condition,

14	MOD_LOPWR	I	"1" or NC = module in low power (safe) mode, "0" = power-on enabled
15	MOD_ABS	O	"1" or NC = module absent, "0" = module present
16	MOD_RSTn	I	"0" = resets the module, "1" or NC = module enabled
17	MDC	1.2V COMS I	Management Data Clock
18	MDIO	1.2V COMS I/O	Management Data I/O bi-directional data
19	PRTADR0	1.2V COMS I	MDIO Physical Port address bit 0
20	PRTADR1	1.2V COMS I	MDIO Physical Port address bit 1
21	PRTADR2	1.2V COMS I	MDIO Physical Port address bit 2
22	VND_IO_C	I/O	Module Vendor I/O C. NC
23	VND_IO_D	I/O	Module Vendor I/O D. NC
24	VND_IO_E	I/O	Module Vendor I/O E. NC
25	GND	Ground	Signal Ground
26	*(MCLKn)*	CML O	For optical waveform testing
27	*(MCLKp)*	CML O	For optical waveform testing
28	GND	Ground	Signal Ground

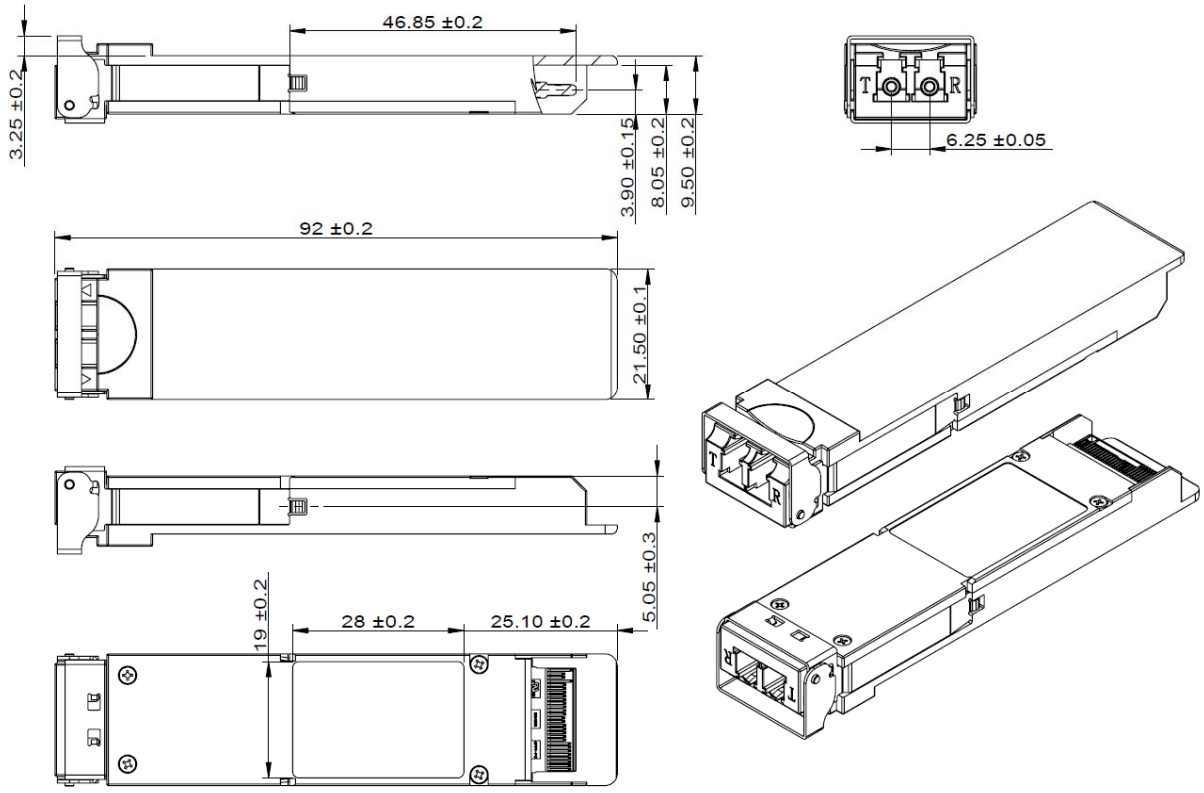
Top Row Pin Descriptions

Pin Num.	Name	Function	Notes
56	GND	Ground	Signal Ground
55	TX3n	Lane 3 Tx Input I	CML Input
54	TX3p		
53	GND	Ground	Signal Ground
52	TX2n	Lane 2 Tx Input I	CML Input
51	TX2p		
50	GND	Ground	Signal Ground
49	TX1n	Lane 1 Tx Input I	CML Input
48	TX1p		
47	GND	Ground	Signal Ground
46	TX0n	Lane 0 Tx Input I	CML Input
45	TX0p		
44	GND	Ground	Signal Ground
43	*(REFCLKn)*	Reference Clock I	Reference Clock Input
42	*(REFCLKp)*		

41	GND	Ground	Signal Ground
40	RX3n	Lane 3 Rx Output O	CML Output
39	RX3p		
38	GND	Ground	Signal Ground
37	RX2n	Lane 2 Rx Output O	CML Output
36	RX2p		
35	GND	Ground	Signal Ground
34	RX1n	Lane 1 Rx Output O	CML Output
33	RX1p		
32	GND	Ground	Signal Ground
31	RX0n	Lane 0 Rx Output O	CML Output
30	RX0p		
29	GND	Ground	Signal Ground

Mechanical Specifications

Parameter	Symbol	Max.	Unit	Spec
Weight		90	g	
Flatness		0.12	mm	CFP MSA CFP4 HW spec Rev.0.1_5.3.1=0.12mm(class=4)
Roughness	Ra	1.6	μm	CFP MSA CFP4 HW spec Rev.0.1_5.3.1=0.16mm(class=4)



LC Connector

*This 2D drawing only for reference, please check with Eoptolink before ordering.

Obtaining Document

You can visit our website: http://www.eoptolink.com
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Revision History

Revision	Initiated	Reviewed	Approved	Revision History	Release Date
V1.a	Oliver	Phlio		Preliminary.	June 15, 2015
V1.b	Oliver			Update Some Projects	Sep 06, 2015
V1.c	Oliver	Phlio	Alex	Update Mechanical , Functional Description and Regulatory Compliance.	Jan 22, 2016
V1.d	Oliver	Angela	Phlio	Update Some Projects	Aug 05, 2016
V1.e	Oliver	Kelly	Phlio	Update Register Description	March 2, 2017

Notice:

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